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EXAMINER	
NGUYEN, PHUONGCHAU BA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,931	PRIMROSE ET AL.	
	Examiner	Art Unit	
	Phuongchau Ba Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5-2-5 election*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) *60-79* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-13,20-25,32-37,44-48 and 55-59* is/are rejected.

7)☒ Claim(s) *2-7,26-31,38-43 and 49-54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 2, 3, 5-10, 14-15, 17-22, 26-34, 38-39, 41-46, 49-50, 52-57 are objected to because of the following informalities: "FIPO" should be changed to ---FIFO--- . Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 25, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Storr (6,633,543).

Regarding claim 1:

Storr (6,633,543) discloses a networking apparatus comprising:

a switching fabric (300) including a plurality of ingress/egress points (not shown) to switch routing paths of packets received through mediums coupled to the ingress/egress points (fig.3),

a first buffering structure (FRM cell processing 311), coupled to a first of said ingress/egress point and a first one of said mediums, including a first FIFO storage structure (314) to stage undiverted ones of a first plurality of egress packets, and first undiverted egress packet drop logic coupled to the first FIFO storage structure to

selectively effectuate head or tail flushes of said first FIFO storage structure (col.7, line 67-col.8, line 9), and

a second buffering structure (RM extract), coupled to a second of said ingress/egress point and a second one of said mediums, including a second FIFO storage structure (316) to stage undiverted ones of a second plurality of egress packets, and second undiverted egress packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure (col.7, line 67-col.8, line 9).

Storr does not explicitly disclose head or tail flushes. However, in the same field of endeavor, Lin (5,764,641) discloses head or tails flushes (beginning of packets-109 in fig.3b or EOP-101 in fig.3a). Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 25:

Storr discloses a networking apparatus comprising:

a switching fabric (300) including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points (fig.3);

a first buffering structure (FRM cell processing 311), coupled to a first of said ingress/egress points and a first of said mediums, including a first FIFO storage structure (314) to stage undiverted ones of a first plurality of ingress packets, and first

undiverted ingress packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flushes of said first FIFO storage structure (col.7, line 67-col.8, line 9), and

a second buffering structure (RM extract), coupled to a second of said ingress/egress points and a second of said mediums, including a second FIFO storage structure (316) to stage undiverted ones of a second plurality of ingress packets, and second undiverted ingress packet drop Logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure (col.7, line 67-col.8, line 9).

Storr does not explicitly disclose head or tail flushes. However, in the same field of endeavor, Lin (5,764,641) discloses head or tails flushes (beginning of packets-109 in fig.3b or EOP-101 in fig.3a). Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 37:

Storr discloses a networking apparatus comprising:

a switching fabric (300) including a plurality of ingress/egress points to switch packets received through mediums coupled to the ingress/egress points (not shown), and

a buffering structure (310) including

a first FIFO storage structure (314), coupled to a first of said ingress/egress points and a first of said mediums, to stage undiverted ones of a first plurality of ingress packets, and undiverted ingress packet drop Logic to selectively effectuate head or tail flushes of said first FIFO storage structure (col.7, line 67-col.8, line 9), and

a second FIFO storage structure (316), coupled to said first ingress/egress point and said first of said mediums, to stage undiverted ones of a first plurality of egress packets, and undiverted egress packet drop Logic to selectively effectuate head or tail flushes of said second FIFO storage structure (col.7, line 67-col.8, line 9).

Storr does not explicitly disclose head or tail flushes. However, in the same field of endeavor, Lin (5,764,641) discloses head or tails flushes (beginning of packets-109 in fig.3b or EOP-101 in fig.3a). Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

3. Claims 9-13, 21-24, 33-36, 45-48, 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Storr (6,633,543) in view of Lin (5,764,641).

Regarding claim 9:

Storr discloses all the claimed limitations, except wherein said first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating

remaining words of the egress packet, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic (CLP= 0 or 1), which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating (discarding) remaining words of the egress packet, to effectuate a head flush of said first FIPO storage structure (fig.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 10:

Storr discloses all the claimed limitations, except wherein said first undiverted egress packet drop Logic comprises first undiverted egress packet read drop Logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first undiverted egress packet drop Logic comprises first undiverted egress packet read

drop Logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure (figs 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 11:

Storr discloses all the claimed limitations, except wherein said first plurality of FIFO storage structures further comprises a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said first plurality of egress packets; and said first associated packet diversion and insertion Logic further includes a diverted egress packet write drop Logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first plurality of FIFO storage structures further comprises a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said first plurality of egress packets; and said first associated packet diversion and insertion Logic further includes a diverted egress packet write drop Logic (CLP logic) coupled to the third FIFO

storage structure to effectuate a tail flush of the third FIFO storage structure (figs.3a-3b, abstract)

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 12:

Storr discloses all the claimed limitations, except wherein said diverted egress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop Logic effectuates a tail flush of the first FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said diverted egress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop Logic effectuates a tail flush of the first FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 13:

Storr discloses all the claimed limitations, except wherein said first buffering structure further comprises a third FIFO storage structure to stage undiverted ones of a

first plurality of ingress packets, and first undiverted ingress packet drop logic to selectively effectuate head or tail flushes of said third FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first buffering structure further comprises a third FIFO storage structure to stage undiverted ones of a first plurality of ingress packets, and first undiverted ingress packet drop logic to selectively effectuate head or tail flushes of said third FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 21:

Storr discloses all the claimed limitations, except wherein said first undiverted ingress packet drop is Logic comprises first undiverted ingress packet read drop Logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the third FIFO storage structure, and if so, invalidating remaining words of the ingress packet to be dropped, to effectuate a head flush of said third FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first undiverted ingress packet drop is Logic comprises first undiverted ingress packet read drop Logic (CLP=0 or 1), which, in response to a drop ingress packet control

signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the third FIFO storage structure, and if so, invalidating (discarding) remaining words of the ingress packet to be dropped, to effectuate a head flush of said third FIPO storage structure (figs.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 22:

Storr discloses all the claimed limitations, except wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop Logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped has already been read out of the third FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said third FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop Logic (CLP logic), which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped has already been read out of the third FIFO storage structure, and if so,

invalidating an EOP indicator of a current word, to effectuate a head flush of said third FIPO storage structure (figs.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 23:

Storr discloses all the claimed limitations, except wherein said first buffering structure comprises a fourth FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets; and diverted ingress packet write drop logic coupled to the fourth FIFO storage structure to effectuate a tail flush of the fourth FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first buffering structure comprises a fourth FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets; and diverted ingress packet write drop logic coupled to the fourth FIFO storage structure to effectuate a tail flush of the fourth FIFO storage structure (figs.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 24:

Storr discloses all the claimed limitations, except wherein said diverted ingress packet write drop Logic effectuates a tail flush of the fourth FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said diverted ingress packet write drop Logic effectuates a tail flush of the fourth FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure (figs.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 33:

Storr discloses all the claimed limitations, except wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop Logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating remaining words of the ingress packet to be dropped, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop logic (CLP= 0 or 1), which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating (discarding) remaining words of the ingress packet to be dropped, to effectuate a head flush of said first FIPO storage structure (figs.3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 34:

Storr discloses all the claimed limitations, except wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (4,764,641) discloses wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped

has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 35:

Storr discloses all the claimed limitations, except wherein said first buffering structure further comprises a third FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets, and diverted ingress packet write drop Logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

However, in the same field of endeavor, Lin (4,764,641) discloses wherein said first buffering structure further comprises a third FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets, and diverted ingress packet write drop logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 36:

Storr discloses all the claimed limitations, except wherein said diverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop logic effectuates a tail flush of the first FIFO storage structure.

However, in the same field of endeavor, Lin (4,764,641) discloses wherein said diverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop logic effectuates a tail flush of the first FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 45:

Storr discloses all the claimed limitations, except wherein said undiverted ingress packet drop Logic comprises undiverted ingress packet read drop Logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating remaining words of the ingress packet to be dropped, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said undiverted ingress packet drop Logic comprises undiverted ingress packet read drop Logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating remaining words of the ingress packet to be dropped, to effectuate a head flush of said first FIPO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 46:

Storr discloses all the claimed limitations, except wherein said undiverted ingress packet drop Logic comprises undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said undiverted ingress packet drop Logic comprises undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol, determines whether a SOP of an ingress packet to be dropped has

already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIPO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 47:

Storr discloses all the claimed limitations, except wherein said buffering structure further comprises a third FIFO storage structure coupled to said first medium to stage diverted ones of said plurality of ingress packets, and diverted ingress packet write drop Logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said buffering structure further comprises a third FIFO storage structure coupled to said first medium to stage diverted ones of said plurality of ingress packets, and diverted ingress packet write drop Logic (CLP logic) coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 48:

Storr discloses all the claimed limitations, except wherein said diverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop Logic effectuates a tail flush of the first FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said diverted ingress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop Logic effectuates a tail flush of the first FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 56:

Storr discloses all the claimed limitations, except wherein said undiverted egress packet drop Logic comprises undiverted egress packet read drop Logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the second FIFO storage structure, and if so, invalidating remaining words of the egress packet, to effectuate a head flush of said second FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) wherein said undiverted egress packet drop Logic comprises undiverted egress packet read drop logic (CLP logic), which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the second FIFO storage structure, and if so, invalidating (discarding) remaining words of the egress packet, to effectuate a head flush of said second FIPO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 57:

Storr discloses all the claimed limitations, except wherein said undiverted egress packet drop Logic comprises undiverted egress packet read drop Logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped has already been read out of the second FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said second FIPO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said undiverted egress packet drop Logic comprises undiverted egress packet read drop Logic, which, in response to a drop egress packet control signal, while operating under a first protocol, determines whether a SOP of an egress packet to be dropped has

already been read out of the second FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said second FIPO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 58:

Storr discloses all the claimed limitations, except wherein said buffering structure further comprises a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said plurality of egress packets; and diverted egress packet write drop Logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said buffering structure further comprises a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said plurality of egress packets; and diverted egress packet write drop Logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

Regarding claim 59:

Storr discloses all the claimed limitations, except wherein said diverted egress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop Logic effectuates a tail flush of the second FIFO storage structure.

However, in the same field of endeavor, Lin (5,764,641) discloses wherein said diverted egress packet write drop Logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop Logic effectuates a tail flush of the second FIFO storage structure. (figs. 3a-3b, abstract).

Therefore, it would have been obvious to an artisan to apply Lin's teaching to Storr's system with the motivation being to prevent partially packets transmitted through the switch.

4. Claims 8, 20, 32, 44, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Storr (6,633,543) in view of Hernandez (6,266,327).

Regarding claim 8:

Storr discloses wherein said first undiverted egress packet drop Logic comprises first undiverted egress packet read drop Logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol (col.7, line 67-col.8, line 9).

Storr discloses all the claimed limitations, except multiplexes an EOP into said first plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Hernandez (6,266,327) discloses multiplexing an EOP into said first plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said first FIPO storage structure (abstract, col.2, line 43-col.3, line 5).

Therefore, it would have been obvious to an artisan to apply Hernandez's teaching to Storr's system with the motivation being to prevent transmitting packets of non-comformance frame thus improving the traffic flow on the switch.

Regarding claim 20:

Storr discloses wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop Logic, which, in response to an underflow condition of said third FIFO storage structure, while operating under a first protocol,

Storr discloses all the claimed limitations, except multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said third FIPO storage structure.

However, in the same field of endeavor, Hernandez (6,266,327) discloses multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said third FIPO storage structure (abstract, col.2, line 43-col.3, line 5).

Therefore, it would have been obvious to an artisan to apply Hernandez's teaching to Storr's system with the motivation being to prevent transmitting packets of non-comformance frame thus improving the traffic flow on the switch.

Regarding claim 32:

Storr discloses wherein said first undiverted ingress packet drop Logic comprises first undiverted ingress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol (col.7, line 67-col.8, line 9).

Storr discloses all the claimed limitations, except multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Hernandez (6,266,327) discloses multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure (abstract, col.2, line 43-col.3, line 5).

Therefore, it would have been obvious to an artisan to apply Hernandez's teaching to Storr's system with the motivation being to prevent transmitting packets of non-comformance frame thus improving the traffic flow on the switch.

Regarding claim 44:

Storr discloses wherein said undiverted ingress packet drop Logic comprises undiverted ingress packet read drop Logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol (col.7, line 67-col.8, line 9).

Storr discloses all the claimed limitations, except multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

However, in the same field of endeavor, Hernandez (6,266,327) discloses multiplexing an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure (abstract, col.2, line 43-col.3, line 5).

Therefore, it would have been obvious to an artisan to apply Hernandez's teaching to Storr's system with the motivation being to prevent transmitting packets of non-conformance frame thus improving the traffic flow on the switch.

Regarding claim 55:

Storr discloses wherein said undiverted egress packet drop Logic comprises undiverted egress packet read drop Logic, which, in response to an underflow condition of said second FIFO storage structure, while operating under a first protocol (col.7, line 67-col.8, line 9).

Storr discloses all the claimed limitations, except multiplexing an EOP into said plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said second FIPO storage structure.

However, in the same field of endeavor, Hernandez (6,266,327) discloses multiplexing an EOP into said plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said second FIPO storage structure (abstract, col.2, line 43-col.3, line 5)

Therefore, it would have been obvious to an artisan to apply Hernandez's teaching to Storr's system with the motivation being to prevent transmitting packets of non-conformance frame thus improving the traffic flow on the switch.

Allowable Subject Matter

5. Claims 2-7, 14-19, 26-31, 38-43, 49-54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 571-272-3148. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 2:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuongchau Ba Nguyen
Examiner
Art Unit 2665

DUC HO
PRIMARY EXAMINER

7-22-05